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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
08/902,133	07/29/97	FORBES L	303.356US1

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EXAMINER	
ECKERT II,G	
ART UNIT	**PAPER NUMBER**
2815	23

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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No. 08/902,133	Applicant(s) Forbes et al.
	Examiner George C. Eckert II	Group Art Unit 2815

☒ Responsive to communication(s) filed on *Jun 28, 2000* .

☒ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) *1-16, 18-20, 28, 29, and 32-78* is/are pending in the application.

Of the above, claim(s) _____ is/are withdrawn from consideration.

☒ Claim(s) *45-48, 53, 54, 59, 60, 67-70, and 73-76* is/are allowed.

☒ Claim(s) *1-6, 8-16, 19, 20, 28, 29, 32-37, 43, 49, 51, 55, 57, 61, 63, 65, 71, 72,* is/are rejected.

☒ Claim(s) *7, 18, 38-42, 44, 50, 52, 56, 58, 62, 64, 66, and 78* is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____ .

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____ .

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). *22*

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

DETAILED ACTION

Response to Amendment

1. Applicant's amendment dated June 28, 2000, in which claims 29, 66, 68 and 70 were amended and claims 73 - 78 newly added, has been placed of record in the file. Claims 1-16, 18-20, 28, 29 and 32-78 are now pending.

Claim Objections

2. Objection to claim 29 has been overcome by Applicant's amendment.

Claim Rejections - 35 USC § 112

3. Rejection of claims 19, 28, 29, 32, 43, 45, 47, 49, 51, 53, 55, 57, 59, 61, 63, 65, 67, 69 and 72 are under 35 U.S.C. 112, second paragraph, is withdrawn.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-6, 8, 9 and 29 are rejected under 35 U.S.C. 102(b) as being anticipated by the article *Amorphous silicon/amorphous silicon carbide heterojunctions applied to memory device*

structures, Sakata et al., Electronics Letters, Vol. 30, No. 9, pp. 688-89, April 1994, (hereinafter Sakata). Sakata teaches a device comprising:

a storage electrode to store charge, formed of amorphous hydrogenated silicon;

a control electrode formed of a metal and separated from the amorphous silicon storage electrode by an intergate dielectric comprised of amorphous hydrogenated silicon carbide. Sakata also teaches that the amorphous silicon carbide has a permittivity (or dielectric constant) of 8 (see Sakata col. 2, at *Results and discussion*) which is higher than the permittivity of silicon dioxide which is 3.9. With regard to claims 1, 2, 6 and 8, Sakata further teach an insulator of graded amorphous hydrogenated silicon carbide adjacent to the storage electrode of amorphous silicon. As taught by Applicant, the inherent electron affinity of silicon is 4.2 eV and that of silicon carbide is 3.24 eV (being greater than silicon dioxide at 0.9 eV) such that the barrier energy is 4.2 - 3.24 or 0.96 eV. With regard to claims 3-5, the limitations of these claims are related to the manner in which the structure of claims 1 and 2 is used or an inherent characteristic of that structure and they do not add further structural limitations to that already claimed. Therefore they are rejected under Sakata. With regard to claim 9, Sakata teaches that the storage electrode formed of amorphous hydrogenated silicon is isolated from conductors and semiconductors as it is formed as a layer sandwiched between layers of amorphous silicon-carbide.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 10-16, 20, 28, 32-37, 43, 49, 51, 55, 57, 61, 63, 65, 71, 72 and 77 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakata in view of Japanese publication 8-255878 to Sugita et al. Sakata has taught the limitations of claim 29 as discussed above but has not expressly disclosed the device having a source region, a drain region or a channel region. However, such limitations are considered obvious in light of that known in the art. Such a device including an insulator formed over a substrate in which a source, drain and channel region therebetween are formed, a floating gate over the insulator, a intergate dielectric over the floating gate, and a control gate over the intergate dielectric is well known in the art as an EPROM device. For example, Sugita et al. teaches such a device in their abstract figure. Such a device has widespread application in the art. Given the advantages of the memory device taught by Sakata, for example that device leakage current is low, and the motivation provided by Sakata that the structure may be used in a floating gate memory device, it would have been obvious to form the device of Sakata having source, drain and channel regions such as those known in the industry and taught by Sugita et al.

Allowable Subject Matter

6. Claims 7, 18, 38-42, 44, 50, 52, 56, 58, 62, 64, 66 and 78 are objected to as being dependent on a rejected base claim but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claims 45-48, 53, 54, 59, 60, 67-70 and 73-76 are allowed. The following is a restatement of reasons for the indication of allowable subject matter: The prior art fails to teach, disclose, or suggest, either alone or in combination, a memory device wherein a storage electrode is formed above an insulator layer such that the barrier energy therebetween is less than approximately 3.3 eV and wherein the storage electrode has an electron affinity smaller than that of polycrystalline silicon, as instantly taught and claimed by Applicant. Nor did the prior art teach a memory device in which the capacitor formed between a floating gate and a control gate had a larger area than did the capacitor formed between the floating gate and a channel region, as instantly taught and claimed by Applicant.

Response to Arguments

7. Applicant's arguments filed June 28, 2000 have been fully considered but they are not persuasive. Regarding the rejections of claims 1-6, 8, 9 and 29 under 35 U.S.C. 102 over Sakata et al., Applicants argue that Sakata is deficient because its hydrogenated amorphous silicon (a-Si:H) layer can not be considered "an electrode" as instantly cited in claim 29. Applicants specifically state that such an a-Si:H layer has a high resistivity in contrast to an "electrode" which, according to Applicants, "is known to those skilled in the art as a continuous, electrically

conductive structure." To distinguish the "electrode" of the instant device over that taught by Sakata, Applicants point to specific material differences by citing pages of the instant specification which teach an "electrode" made of polysilicon or silicon carbide.

To begin, the instant claim merely cites "a storage electrode to store charge" but does not cite additional structural or material limitations to be satisfied. As such, the claim stands properly rejected without finding a specific material property in the reference. Alternatively, the argument that the term "storage electrode" by itself must always carry with it a specific material property or physical structure cannot be maintained. It is acknowledged that the term "electrode" is used widely in the art and typically connotes a low resistance electrical connection. However, the term does not carry such weight in the instant claim because it is not being used as an "electrode" in the general sense. Rather, the claim states, and the disclosure supports, a "*storage* electrode" (emphasis added). As is known in the art and as used in the instant device, such a storage electrode has no physical connection to any other conductive component which establishes a low resistance electrical path as would an "electrode." Rather, as its name implies, the "floating" gate is electrically connected to nothing, but is only floating. As such, using the term "storage electrode" does not bring with it any specific characteristic as Applicants suggest.

In light of the term "storage electrode" then, certainly it must be agreed to by Applicants that Sakata discloses such a component, especially in light of Sakata's teaching that "both electrons and holes are *stored* in the a-Si:H layer." (Emphasis added). Sakata, column 2, *Results*

and discussion. On its face then, Sakata clearly does teach such a "storage electrode to store charge."

Even considering Applicant's argument that a specific material difference is imputed by the term "storage electrode" such that the materials used by Applicants differentiate over Sakata, such argument is not deemed persuasive. Applicants indicate that the instant "storage electrode" is made of either polysilicon or silicon carbide. However, no other teachings are provided by Applicant which refine the widely variable properties of these materials such that they are not anticipated by Sakata. Indeed, Sakata teaches the functional equivalent of a polysilicon or silicon carbide storage electrode by using a-Si:H.

Regarding Applicant's use of polycrystalline silicon, Sakata also teaches the use of silicon but in an hydrogenated and amorphous form. Sakata further teaches that the a-Si:H is not doped. Applicants have implied a characteristic difference between such crystallinities in that the a-Si:H layer of Sakata has a high resistivity. Such is acknowledged. However, Applicants have not sufficiently taught their device, and moreover have not claimed it, such that their layer of polysilicon would not also have a high resistivity. For example, Applicants have nowhere stated the necessity to dope the polysilicon to achieve a lower resistance. And, like a-Si:H, if polysilicon is left intrinsic, it too will have a high resistance. See for example US 4,462,150 to Nishimura et al. and US 4,768,072 to Seki et al. Nishimura teaches intrinsic polysilicon has a resistivity of more than 10^9 ohms while Seki teaches intrinsic a-Si:H has a resistivity of 10^{11} - 10^{12} ohms. These resistivities are sufficient to consider both crystallinity types as insulators.

A similar argument can be made regarding the use of silicon carbide. Applicants teach that the silicon carbide may be micro- or poly-crystalline (p. 11, lines 16-17) but do not give additional information or indicate the necessity for doping such that a specific resistance is achieved. And while it is acknowledged that hydrogenated amorphous silicon as used by Sakata has a high resistance, the various forms of silicon carbide also have a high resistance. See for example US 6,075,259 to Baliga which teaches resistivity of intrinsic silicon carbide as high as 10^{16} ohms.

Applicants finally argue that the operation of Sakata's device is based on "pure speculation" and state that such speculation must negate the teaching of an "electrode." This argument is without merit as it is not clear where the requirement has been made that a reference may not be speculative as to the explanation of an aspect of its teachings. As stated above, 35 U.S.C. 102(b) indicates that an application for patent will be granted unless "the invention was... described in a printed publication in this . . . country . . .more than one year prior to the date of application for patent in the United States." Because Applicants invention was described in a printed publication more than one year prior to the application, Applicants argument regarding speculation is not considered persuasive.

The remaining claims were rejected under 35 U.S.C. 103 which Applicants traverse. Specifically, Applicants state that the use of Sakata is not sufficient for the rejection because Sakata does not teach a floating gate nor source/drain regions. That Sakata does teach a floating gate electrode was discussed above and will not be repeated. That Sakata does not expressly

disclose source/drain regions is acknowledged. However, source/drain regions are known in the art and taught by Sugita as made clear in the previous rejection.

Applicants argument turns on a lack of motivation to combine Sakata and Sugita, primarily because of the speculative nature of Sakata. However, Applicants arguments are not persuasive because motivation was found in the references and established in the rejection. Specifically, Sakata teaches a memory device which they state "can be applied to electrically programmable and erasable memory devices[.]" Such devices, known as EPROMs, are well known in the art and use sources and drains to electrically communicate and function with external devices. Sugita teaches a similar EPROM and shows the device having source and drain regions. That Sugita's "traditional" floating gate is made of a material different from that taught by Sakata is not enough to negate the obviousness rationale as made in the rejection. Nor is it enough to state that the operation of the two devices may be different. Sugita's is a traditional device with well known operation while Sakata et al. have speculated on the reason for their device's operation. However, both devices are sufficiently similar in nature that such an apparent and minor distinction will not negate their combination. Both teachings are of semiconductor devices, used as memory devices, using floating gates to store charge in a storage electrode. The arguments are not persuasive and the rejection is maintained.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to George C. Eckert II whose telephone number is (703) 305-2752.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

Mahshid Saadat
Supervisory Patent Examiner
Technology Center 2800

GCE

September 13, 2000